What is claimed is:

1	1.	A voltage-level converter comprising:
2		a static voltage-level converter; and
3		a split-level output circuit coupled to the static voltage-level converter.
1	2.	The voltage-level converter of claim 1, wherein the static voltage-level converter
2	compr	rises:
3		an input node, a first output node, and a second output node;
4		a first pair of transistors connected in series, the first pair of transistors including a
5	first tr	ansistor and a second transistor, the first transistor coupled to the input node;
6		a second pair of transistors connected in series, the second pair of transistors
7	includ	ing a first transistor and a second transistor, the second transistor of the second pair
8	of tran	nsistors being cross-coupled with the second transistor of the first pair of transistors
9	and th	e second transistor of the second pair of transistors being coupled to the first output
10	node;	and
11		an inverter coupled to the input node, to the first transistor of the second pair of
12	transi	stors, and to the second output node.
1	3.	The voltage level converter of claim 2, wherein the split-level output circuit
2	comp	rises a plurality of insulated-gate field-effect transistors.

- comprises a plurality of insulated-gate field-effect transistors.
- The voltage-level converter of claim 1, wherein the static voltage-level converter 1 4.
- comprises a first output node and a second output node and the split-level output circuit 2
- comprises a first split-level input node, a second split-level input node, a split-level 3
- output node, a first insulated-gate field-effect transistor (FET) coupled to the first split-4
- level input node and a second insulated-gate FET coupled to the second split-level input 5
- node, the first insulated-gate FET being connected in series with the second insulated-6
- gate FET, the first insulated gate FET and the second insulated gate FET having a 7

- 8 common node coupled to the split-level output node and the first split-level input node
- 9 coupled to the first output node and the second split-level input node coupled to the
- second output node.
- 1 5. The voltage-level converter of claim 4, wherein the first insulated-gate field-effect
- 2 transistor comprises a p-type insulated-gate field-effect transistor.
- 1 6. The voltage-level converter of claim 5, wherein the second insulated-gate field-
- 2 effect transistor comprises an n-type insulated gate field-effect transistor.
- 1 7. A voltage-level converter comprising:
- a static voltage-level converter including an input node, a first pull-up node, a
- 3 second pull-up node, an inverter output node, and an output node;
- a first transistor coupled to the input node and the first pull-up node; and
- a second transistor coupled to the second pull-up node and the inverter output
- 6 node.
- 1 8. The voltage-level converter of claim 7, wherein the first transistor comprises an
- 2 insulated gate field-effect transistor and the second transistor comprises an insulated-gate
- 3 field-effect transistor.
- 1 9. The voltage-level converter of claim 7, wherein the first transistor comprises a p-
- 2 type insulated-gate field-effect transistor and the second transistor comprises a p-type
- 3 insulated-gate field-effect transistor.
- 1 10. The voltage-level converter of claim 9, further comprising:
- 2 an inverter coupled to the output node.

- 1 11. The voltage-level converter of claim 10, wherein the inverter comprises: 2 a single-input inverter. 1 12. The voltage-level converter of claim 11, wherein the inverter comprises: 2 an n-type insulated-gate field-effect transistor coupled to the output node; 3 a first p-type insulated-gate field-effect transistor coupled to the inverter output 4 node; 5 a second p-type insulated-gate field-effect transistor coupled to the static level 6 converter, wherein the n-type insulated-gate field-effect transistor, the first p-type insulated-gate field-effect transistor, and the second p-type insulated-gate field-effect 7 8 transistor are connected in series. 1 13. A voltage-level converter comprising: 2 a static voltage-level converter having an input node and an output node; 3 a first transistor coupled to the input node and the static voltage-level converter; 4 and 5 a second transistor coupled to the static voltage-level converter. 1 14. The voltage-level converter of claim 13, wherein the first transistor comprises a p-2 type insulated-gate field-effect transistor.
- 1 15. The voltage-level converter of claim 14, wherein the second transistor comprises a
- 2 p-type insulated-gate field-effect transistor.
- 1 16. The voltage-level converter of claim 15, further comprising:
- 2 an inverter coupled to the output node.
- 1 17. The voltage-level converter of claim 16, wherein the inverter comprises a single-
- 2 input inverter.

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- 1 18. The voltage-level converter of claim 16, wherein the inverter comprises:
- a multiple-input inverter coupled to at least three outputs of the static voltage-
- 3 level converter.
- 1 19. A voltage-level converter comprising:
- a static voltage-level converter comprising an input node, an output node, a first
- 3 pair of serially connected transistors, a second pair of serially connected transistors, and
- 4 an inverter coupled between the first pair of serially connected transistors and the second
- 5 pair of serially connected transistors;
- a first transistor located between the first pair of serially connected transistors and
- 7 coupled to the input node; and
- 8 a second transistor located between the second pair of serially connected
- 9 transistors and coupled to the inverter.
- 1 20. The voltage-level converter of claim 19, wherein the first transistor comprises an
- 2 insulated-gate field-effect transistor.
- 1 21. The voltage-level converter of claim 20, wherein the second transistor comprises
- 2 an insulated-gate field-effect transistor.
- 1 22. The voltage-level converter of claim 21, further comprising:
- a buffer coupled to the output node.
- 1 23. The voltage-level converter of claim 22, wherein the buffer comprises a single-
- 2 input inverter.

1	24. The voltage-level converter of claim 22, wherein the buffer comprises:	
2	a multiple-input inverter coupled to at least three outputs of the static voltage-	
3	level converter.	
1	25. The voltage-level converter of claim 24, wherein the multiple-input inverter ha	เร
2	an inverter output node and comprises:	
3	an n-type insulated-gate field-effect transistor;	
4	a first p-type insulated-gate field-effect transistor; and	
5	a second p-type insulated-gate field-effect transistor, wherein the n-type insula	ted-
6	gate field-effect transistor, the first p-type insulated-gate field-effect transistor, and the)
7	second p-type insulated-gate field-effect are connected in series and the n-type insulate	ed-
8	gate field-effect transistor is coupled to the inverter output node, the first p-type	
9	insulated-gate field-effect transistor is coupled to the first pair of serially connected	
10	transistors, and the second p-type insulated-gate field-effect transistor is coupled to the	3
11	inverter output node.	
1	26. A logic unit comprising:	
2	one or more first logic units adapted to operate at a first voltage;	
3	one or more second logic units adapted to operate at a second voltage, the second	nd
4	voltage being greater than the first voltage; and	
5	a voltage-level converter for coupling at least one of the one or more first logic	;
6	units to at least one of the one or more second logic units, the voltage-level converter	
7	comprising:	
8	a first voltage-level converter comprising an input node coupled to the	at
9	least one of the one or more first logic units, an output node coupled to the at l	east
10	one of the one or more second logic units, an inverter output node, a first pair of	of
11	serially connected transistors, and a second pair of serially connected transistor	rs;
12	and	

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13	a first transistor located between the first pair of serially connected	ı		
14	transistors and coupled to the input node; and			
15	a second transistor located between the second pair of serially con-	nected		
16	transistors and coupled to the inverter output node.			
1	27. The voltage-level converter of claim 26, wherein the first transistor compa	rises a		
2	first insulated-gate field-effect transistor and the second transistor comprises a sec	cond		
3	insulated-gate field-effect transistor.			
1	28. The voltage-level converter of claim 27, wherein the first insulated-gate fi	ield-		
2	effect transistor comprises a p-type insulated-gate field-effect transistor and the second			
3	insulated-gate field-effect transistor comprises a p-type insulated-gate field-effect			
4	transistor.			